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R. Alan Burnett
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025-1026

EXAMINER

CHAN, EDDIE P

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,943	STARK ET AL. <i>[Signature]</i>	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12 February 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 12/28/2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
.Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of the following papers:
 - 1) Amendment B (2/12/04)
2. Claims 1-20 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1-12, 15-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Simar, Jr. et al. (US006182203B1).

5. **In regard to claim 1:**
6. Simar et al. disclose a processing machine (fig. 1) comprising a:
 - a) a data memory (fig. 1, element 3);

b) a control engine (fig. 1, the program fetch unit 7a, instruction dispatch unit 7b, instruction decode unit 7c, control registers 10a, and control logic 10b) linked in communication with the data memory (fig. 1, linked via the data path);

c) an instruction memory (fig. 1, program memory 2), in which instructions may be stored, having an input for receiving control information from the control engine (fig. 1, communication link 'a' between program memory and program fetch);

d) a plurality of coprocessors (fig. 1, functional units (FU) 12a1-12a4, 12b1-12b4), each connected in communication with the data memory and the control engine, each of said control engine and plurality of coprocessors being enabled to perform simultaneous functions in response to a single instruction (the control engine elements control registers 10a and the control logic 10b control the execution of all the instructions [col. 7 lines 5-6; col. 8 lines 37-43] and all of the functional units execute the instructions simultaneously in response to a single Very Long Instruction Word (VLIW) [col. 4 lines 64-67; col. 5 line 1; col. 33, lines 46-49]. Thus the control engine and the functional units perform the functions of controlling and executing simultaneously in response to a single VLIW instruction respectively).

7. In regard to claim 2:

8. Simar et al. do not explicitly disclose that the control engine comprises a microcontroller. However, the control registers (fig. 1, 10a) and control logic (fig. 1, 10b) of the control engine perform the function of controlling various processor operations

(col. 7 lines 5-6) and hence are a controller of the microchip. Thus it is deemed inherent to the processor of Simar et al. that the control engine comprises a microcontroller.

9. In regard to claim 3:

10. Simar et al. further disclose a main memory (fig. 23, external memory interface indicates the presence of a main memory) linked in communication with at least one of said plurality of coprocessors (fig. 23, FU D2 is connected to the main memory via a data memory interface, data memory controller and an external memory interface).

11. In regard to claim 4:

12. Simar et al. further disclose that the said at least one coprocessor comprises a bus interface coprocessor (fig. 23, FU D2 comprises a bus interface coprocessor as it is interfaces with the memory bus).

13. In regard to claim 5:

14. Simar et al. further disclose that the processing machine is used to perform a particular task (execute a program) and wherein each coprocessor (FU) is designated to perform at least one specific subtask of that particular task (each FU executes a specific operation or subtask of the program [col. 7 table 1])

15. In regard to claim 6:

16. Simar et al. further disclose that the particular task (program) comprises processing a data manipulation algorithm (data encryption, col. 85, table 54), and specific subtasks performed by separate coprocessors include a memory bus interface function (fig. 23, FU D2 comprises a bus interface coprocessor as it interfaces with the memory bus) and a data processing algorithm function (FU S performs 32-bit arithmetic operations, col. 7, table 1).

17. In regard to claim 7:

18. Simar et al. further disclose that the data processing algorithm comprises an encryption algorithm (data encryption, col. 85, table 54).

19. In regard to claim 8:

20. Simar et al. disclose a processing machine (fig. 1) comprising:

- a) a data memory (fig. 1, element 3);
- b) a main memory (fig. 23, external memory interface indicates the presence of a main memory);
- c) a microcontroller (fig. 1, the program fetch 7a, instruction dispatch 7b, instruction decode 7c, control registers 10a, and control logic 10b are a controller of the microchip), linked in communication with the data memory (fig. 1, linked via the data path);
- d) an instruction memory (fig. 1, program memory 2), in which instructions may be stored, having an input for receiving control information from the

microcontroller (fig. 1, communication link 'a' between program memory and program fetch), the microcontroller having an input to receive instructions from the instruction memory (fig. 1, program fetch 7a of the microcontroller inputs instructions from the instruction memory);

e) a first coprocessor providing a bus interface function (fig. 23, FU D2 provides a bus interface function as it is interfaces with the memory bus) when operational, linked in communication with each of the main memory (fig. 23, FU D2 is connected to the main memory via a data memory interface, data memory controller and an external memory interface), the data memory (fig. 1, communication link 'b' between D2 and data memory), and the microcontroller (fig. 1), and having an input to receive instructions from the instruction memory (col. 6 lines 64-67, an instruction is fetched from the instruction memory, decoded, and sent to the FU D2); and

f) a second coprocessor (FU M2), linked in communication with the data memory (fig. 1, via the register file and FU D2) and the microcontroller (fig. 1) and having an input to receive instructions from the instruction memory (col. 6 lines 64-67, an instruction is fetched from the instruction memory, decoded, and sent to the FU M2), wherein the data memory, the microcontroller, the instruction memory, and the first and second coprocessors are coupled in parallel (Although this feature is not explicitly shown all of these elements must be connected to a clock network in parallel to receive a clock signal at the same time. Therefore it is

deemed inherent to the design that these elements are coupled in parallel with the clock network so that they can operate in lockstep).

21. In regard to claim 9:

22. Simar et al. further disclose a third coprocessor (FU S2) linked in communication with the data memory (fig. 1, via the register file and FU D2) and the microcontroller (fig. 1) and having an input to receive instructions from the instruction memory (col. 6 lines 64-67, an instruction is fetched from the instruction memory, decoded, and sent to the FU S2).

23. In regard to claim 10:

24. Simar et al. further disclose a third coprocessor (FU L2) linked in communication with the data memory (fig. 1, via the register file and FU D2) and the microcontroller (fig. 1) and having an input to receive instructions from the instruction memory (col. 6 lines 64-67, an instruction is fetched from the instruction memory, decoded, and sent to the FU L2).

25. In regard to claim 11:

26. Simar et al. further disclose that each of the first and second coprocessors and the microcontroller perform simultaneous coordinated functions in response to a single instruction issued from the instruction memory (all of the functional units execute instructions simultaneously in response to a single Very Long Instruction Word (VLIW)

[col. 4 lines 64-67; col. 5 line 1; col. 33, lines 46-49] issued from the program memory [fig. 1, element 2]).

27. In regard to claim 12:

28. Simar et al. further disclose that the second coprocessor is enabled to process a data manipulation algorithm (FU M2 performs 16 X 16 bit multiplies, col. 7, table 1).

29. In regard to claim 15:

30. Simar et al. disclose a method of processing a data manipulation task (a program) with a processing machine (fig. 1) including a control engine (fig. 1, the program fetch unit 7a, instruction dispatch unit 7b, instruction decode unit 7c, control registers 10a, and control logic 10b) and a plurality of coprocessors (fig. 1, functional units (FU) 12a1-12a4, 12b1-12b4) coupled in parallel (Although this feature is not explicitly shown all of these elements must be connected to a clock network in parallel to receive a clock signal at the same time. Therefore it is deemed inherent to the design that these elements are coupled in parallel with the clock network so that they can operate in lockstep), comprising:

- 1) dividing the data manipulation task into a plurality of subtasks (a program is divided into a plurality of instructions);
- 2) issuing a sequence of instructions (VLIWs) having a plurality of portions (have up to 8 instructions, col. 33, lines 46-49) to the control engine and each of said plurality of coprocessors (issued to the program fetch unit [fig. 1, 7a] and the

functional units [col. 33 lines 44-50] from the program memory [fig. 1, element 2]);

3) performing separate subtasks with the control engine (control registers 10a and the control logic 10b perform control operations in response to instructions of the VLIW [col. 7 lines 5-6; col. 8 lines 37-43]) and each of said plurality of coprocessors (the FUs perform the execution of the instructions of the VLIW [col. 4 lines 64-67; col. 5 line 1; col. 33, lines 46-49]) in response to corresponding portions of the instructions received by each of these components;

4) coordinating an execution of each portion of instructions (instructions of Very Long Instruction Word (VLIW) [col. 33 lines 46-49]) received by the control engine (fig. 1, program fetch unit [7a] of control engine receives the instruction) and each of said plurality of coprocessors (fig. 1, FUs 12a and 12b) such that the subtasks performed by these components are performed substantially in parallel. (control registers [10a] and the control logic [10b] of the control engine perform the subtask of control [col. 7 lines 5-6; col. 8 lines 37-43] and all of the functional units perform the subtask of executing the instructions **in parallel** in response to the VLIW [col. 4 lines 64-67; col. 5 line 1; col. 33, lines 46-49]).

31. In regard to claim 16:

32. Simar et al. further disclose that the coordination of the execution of the portions of instructions (instructions of Very Long Instruction Word (VLIW) [col. 33 lines 46-49]) is performed by the control engine via execution control signals sent to each of said

plurality of coprocessors (control registers [10a] and the control logic [10b] of the control engine perform the subtask of control [col. 7 lines 5-6; col. 8 lines 37-43] and fig. 2 shows control signals going from the control register file to the FUs).

33. In regard to claim 17:

34. Simar et al. do not explicitly mention the limitations of the processing machine comprises a programmed state machine and wherein each of the control engine and said plurality of coprocessors is caused to cycle through a respective set of machine states in response to instruction portions received by that component. However, the control engine and the plurality of coprocessors (FUs) are programmed to repeatedly go through the machine states of fetch, dispatch, decode, and execute in response to a particular instruction hence making it inherent to the VLIW processor of Simar et al. that the control engine and plurality of coprocessors cycle through a respective set of machine states in response to instruction portions received by that component which substantiates that the VLIW processor comprises a programmed state machine.

35. In regard to claim 18:

36. Simar et al. further disclose that one of the subtasks comprises a bus interface function (fig. 23, FU D2 performs the subtask of a bus interface function as it is shown to interface with the memory bus).

37. In regard to claim 19:

38. Simar et al. do not explicitly disclose that the control engine comprises a microcontroller. However, the control registers (fig. 1, 10a) and control logic (fig. 1, 10b) of the control engine perform the function of controlling various processor operations (col. 7 lines 5-6) and hence are a controller of the microchip. Thus it is deemed inherent to the processor of Simar et al. that the control engine comprises a microcontroller.

39. In regard to claim 20:

40. Simar et al. do not explicitly mention that each instruction is issued from the instruction memory in response to an address sent to the instruction memory from the control engine. However, the program fetch unit (fig. 1, 7a) is in direct communication with the program memory (instruction memory) and receives instructions from the instruction memory. But in order to receive the instruction it requires from the instruction memory an address of the instruction must be sent first. Hence it is deemed inherent to the processor of Simar et al. to issue each instruction from the instruction memory in response to an address sent to the instruction memory from the control engine.

Claim Rejections - 35 USC § 103

41. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

42. Claims 13 and 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Simar et al. (US006182203B1) in view of Bailey et al. ().

43. **In regard to claim 13:**

44. Although Simar et al. mentions that it is an application of the VLIW processor to perform X.25 packet switching (col. 85, table 54) and that the third coprocessor (FU-S) is in communication with the data memory (fig. 1, via register file and FU-D), it differs from the present invention as it does not explicitly disclose that the third coprocessor is enabled to perform an ATM data transfer interface function.

45. Bailey et al. teach that ATM can support X.25 traffic (col. 2, lines 9-12).

46. One of ordinary skill in the art at the time of the invention would have been motivated to perform ATM packet switching using the 3rd coprocessor to transfer the ATM data as it is already in communication with the data memory.

47. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to enable the third coprocessor to perform an ATM data transfer interface function.

48. In regard to claim 14:

49. Although Simar et al. mentions that it is an application of the VLIW processor to perform X.25 packet switching (col. 85, table 54), that the third coprocessor (FU-S) is in communication with the data memory (fig. 1, via register file and FU-D), and that the fourth coprocessor (FU-L) does compare operations (col. 7, table 1) it differs from the present invention as it does not explicitly disclose that the third coprocessor is enabled to perform an ATM data transfer interface function and the fourth coprocessor is enabled to perform an ATM Adaptation Layer (AAL) function.

50. Bailey et al. teach that ATM can support X.25 traffic (col. 2, lines 9-12). They also teach that the AAL functions include segmentation, reassembly, error detection, and message identification multiplexing (col. 5, lines 38-40) which are used in packet switching.

51. One of ordinary skill in the art at the time of the invention would have been motivated to perform ATM packet switching using the 3rd coprocessor to transfer the ATM data as it is already in communication with the data memory and the 4th coprocessor to perform an AAL function such as error detection by compare operations.

52. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to enable the third coprocessor to perform an ATM data transfer interface function and enable the fourth coprocessor to perform an ATM Adaptation Layer function.

Response to Arguments

53. Applicant's arguments filed 2/12/04 paper number 6 have been fully considered but they are not persuasive.

54. On pages 9 and 10 Applicant argues in essence:

"Simar fails to disclose a control engine and coprocessors to perform simultaneous functions in response to a single instruction ... fails to disclose both a control engine and coprocessors receiving portions of a single instruction ... fetch unit 7a, dispatch unit 7b, and decode unit 7c are earlier in the data path and therefore do not perform simultaneous functions with the functional units in response to a single instruction."

55. However, Simar does teach a control engine and coprocessors performing simultaneous functions in response to a single instruction. The control engine does not only comprise of fetch unit 7a, dispatch unit 7b, and decode unit 7c, but also the control registers 10a and control logic 10b. These control elements 10a and 10b control the execution of the single VLIW instruction [col. 7, lines 5-6; col. 8, lines 37-48] simultaneously with the functional units that actually execute it. This is because control of the instruction must be done along with the execution. Also, the argument made that Simar fails to disclose both a control engine and coprocessors receiving portions of a single instruction is inappropriate because the claim nowhere calls for the control engine and the functional units to **receive** portions of a single instruction.

56. On page 10 Applicant argues in essence:

"Simar illustrates program fetch 7a, dispatch unit 7b, and decode unit 7c as coupled in series with functional units...Simar fails to disclose each and every element of claims 8 and 15..."

57. The claim language in claim 8 calls for the data memory, the instruction memory, and the first and second coprocessors are coupled in parallel and in claim 15 that the control engine and the coprocessors are coupled in parallel. However, because claim language is not limited to having these elements coupled in parallel **with each other** and can be coupled in parallel with something else, it is broad enough to read on these elements being coupled in parallel to the inherent clock network in order to receive a clock signal at the same time so that they can operate in lockstep.

Conclusion

58. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AVG
amol.gole@uspto.gov

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Eddie Chan
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100